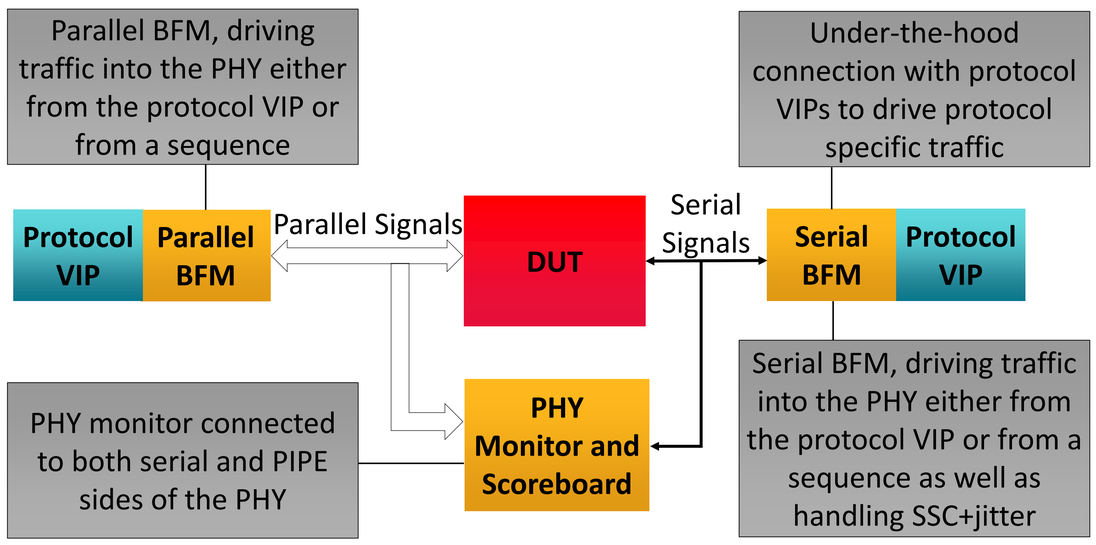
PHY Verification IP

Analysis

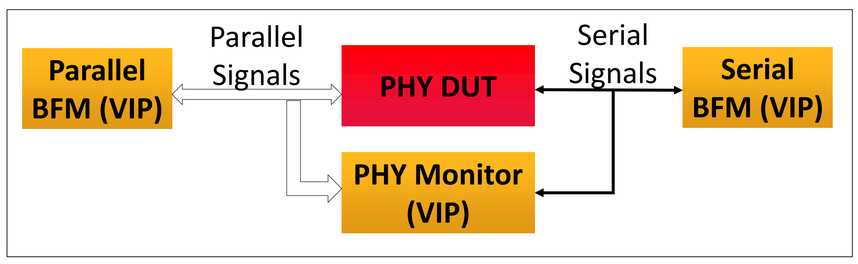
In industry there was no solution to verify standalone PIPE interface based PHY design. Customers have been verifying their PCIe, USB, USB4 PIPE PHY designs using protocol VIPs or custom traffic generators, which introduced an overhead to the verification in the form of protocol specific rules that were outside the scope of the PHY. Also, there was no PHY monitor solution which can observe serial and parallel interface of the PHY DUT. We have developed a VIP solution to address this gap to verify standalone PHY DUT design.

PHY Verification Architecture

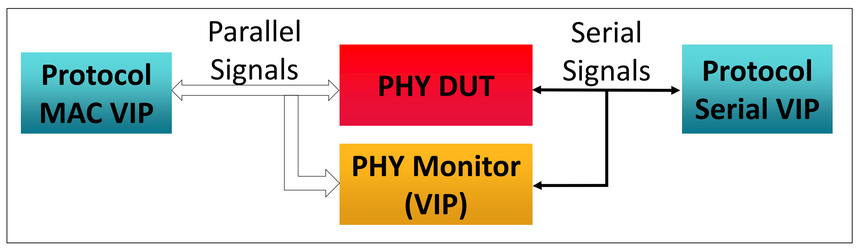


PHY VIP Use Models

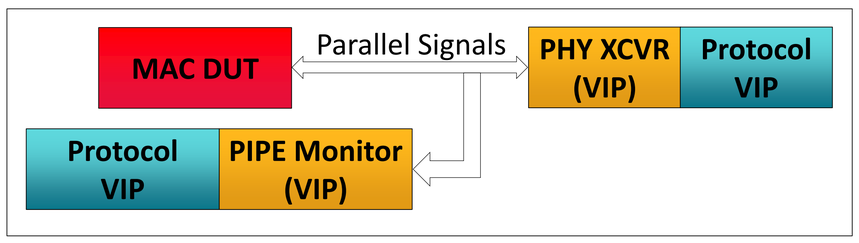
- **PHY DUT environment** where traffic is driven by the PHY BFM on both serial and PIPE side.



- **Monitor only environment** where the PHY monitor is added on top of protocol VIPs, where MAC VIP and Serial VIP are having their own pipe and serial interface respectively

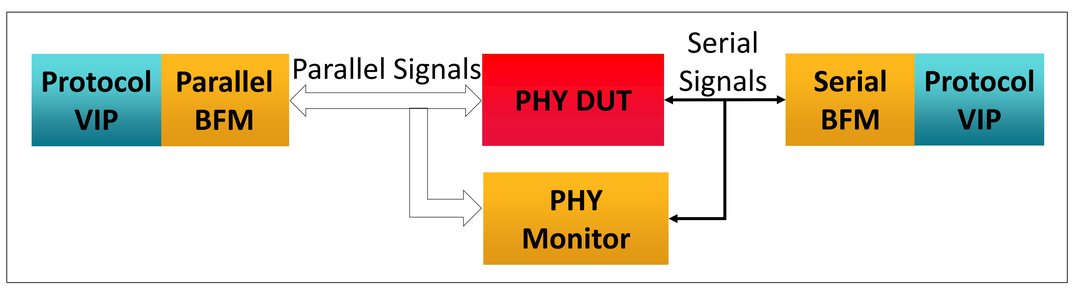


- MAC DUT environment **without having serial interface env.**



PHY VIP Use Models

- **Protocol + PHY VIP integrated environment** for PHY DUT verification, where Parallel BFM and Serial BFM are generic PHY VIP components.



PHY VIP Unique Capabilities

- PIPE specification is fully mapped and annotated with all possible cover groups. User can enable/Disable PHY VIP features statically as well as dynamically.
- PHY monitor was designed for PHY DUTs and therefore allows built in support of features that previously were not supported or required complex testbench code. PHY monitor provides built in data scoreboarding which is flexible enough to support various scenarios such as consuming data due to bit/symbol/block lock, phy delays, etc.

```
/*********************** Tx Path Score Board Summary **********************/
    Number of symbols matched: 1899
    Number of mismatch errors: 0
    Number of symbols uncompared: PIPE side: 0, Serial side: 0
    Number of skip symbols received: PIPE side: 0, Serial side: 0
    Number of skip ordered sets received: PIPE side: 0, Serial side: 0
    Pipe Line Delay: 12 Symbols
    /*****************************************************************************/
```

- Through 200+ end-to-end checkers PHY monitor ensures that the actions on the pipe interface are handled in a timely manner on the serial interface and vice versa.

```
   DENALI_PIPEPHY_NON_IDLE_LINES_AFTER_TXELECIDLE_SET = 117, // PIPE spec Table 6.2 : Tx D
p/Dn lines are not idle even %s after TxElecIdle signal is asserted at %s.Program the exp
ected PHY Delay value using SOMA Parameter :tTxElecIdleResp or Register: DENALI_PIPEPHY_R
EG_TXELECIDLE_RESP_TIME.
```

Results

- To verify PHY DUT, customers were using PCIe or USB3 or USB4 protocol VIPs. With our standalone PHY VIP solution customer can plug their PHY DUT without using any protocol VIPs and they can drive interface signals as per their verification needs and verify their PHY DUT separately. Once their PHY DUT is verified separately with our PHY VIP solution, they can plug the protocol VIPs on top of the PHY VIP to verify PHY DUT more exhaustively.
- Initially with the protocol VIPs, the PHY DUT verification was more tedious and time consuming as customers must make sure of protocol specific rules. With PHY VIP approach, we observed that customers were able to close their PHY DUT verification cycle quickly.
- We have created a separate component called PHY XCVR which provides a direct parallel connection between MAC and protocol VIP. With this solution we have seen around **70%** improvement in test case simulation time.

Conclusion

- PHY VIP solution provides features like built in scoreboard, SSC, Jitter, clock data recovery, PHY specific coverage, reduced verification effort, better performance and speeding up regression closure. With our PHY VIP solution customers can verify their PHY DUT for any protocol without really using a protocol VIP. Our solution also allows the user to extend their verification env to include full protocol stack once their standalone PHY design is fully verified. Many of our customers are using our PHY VIP solution as it is compatible with different PHY modes like PCIe, USB3, USB4.

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